WHAT IS CLAIMED IS:

1. A semiconductor arrangement in which one bump electrode having two protrusions is bonded to an IC electrode on a circuit forming surface of a semiconductor element by a method comprising operating a bonding capillary at a ball bond forming position to form a ball bond portion on the IC electrode, moving the bonding capillary upward with respect to the IC electrode, moving the bonding capillary sideways and then downward with respect to the IC electrode, bonding a wire to the ball bond portion, and cutting the wire, the wire being prevented from coming in contact with portions around the ball bond portion other than the ball bond portion itself by presetting a descent position of the bonding capillary to a position higher than the ball bond forming position; and

wherein said two protrusions are brought in contact with or put close to one electrode on a circuit board when the semiconductor element is mounted on the circuit board.

2. A semiconductor arrangement as claimed in Claim 1, wherein the electrode on the circuit board and said bump electrode are electrically connected to each other.

3. A semiconductor arrangement as claimed in Claim 1, wherein no space is circumscribed by the wire and ball bond portion.

4. A semiconductor arrangement in which a bump electrode is bonded to an IC electrode on a circuit forming surface of a semiconductor element by a method comprising operating a bonding capillary at a ball bond forming position to form a ball bond portion on the IC electrode, moving the bonding capillary upward with respect to the IC electrode, moving the bonding capillary sideways and then downward with respect to the IC electrode, bonding a wire

to the ball bond portion, and cutting the wire, the wire being prevented from coming in contact with portions around the ball bond portion other than the ball bond portion itself by presetting a descent position of the bonding capillary to a position higher than the ball bond forming position;

wherein said bump electrode comprises:

a first protrusion which is comprised of a portion formed by once melting and solidifying a wire and its periphery and is bonded to said IC electrode; and

a second protrusion which is formed of an unmelted portion of said wire and extended from said first protrusion beyond a planar area defined by projecting said first protrusion to a height approximately equal to that of said first protrusion with respect to said IC electrode; and

wherein said first protrusion and said second protrusion are brought in contact with or put close to one electrode on a circuit board when the semiconductor element is mounted on the circuit board.

5. A semiconductor arrangement as claimed in Claim 4, wherein said first protrusion is provided with a formed portion formed by forming a melted portion of said wire by a capillary and solidifying the same and a wire material portion which is comprised of the wire in a vicinity of said melted portion, extended from a vertex portion of said formed portion downwardly of said vertex portion and bonded to said formed portion.

6. A semiconductor arrangement as claimed in Claim 5, wherein said wire material portion extended downwardly from said vertex portion is bonded to said electrode, instead of said formed portion.

7. A semiconductor arrangement as claimed in Claim 4, wherein

said formed portion has a base portion bonded to said electrode and a protruding portion provided upright on said base portion.

8. A semiconductor arrangement as claimed in Claim 4, wherein said second protrusion extends toward an outer end surface side of said semiconductor element without exceeding said outer end surface.

9. A semiconductor arrangement as claimed in Claim 4, wherein said second protrusion extends outwardly of said semiconductor element beyond an outer end surface of said semiconductor element.

10. A semiconductor arrangement as claimed in Claim 4, wherein said first protrusion and said second protrusion have respective flat surface portions at the vertex portions of the protrusions.

11. A semiconductor arrangement as claimed in Claim 4, wherein no space is circumscribed by the wire and ball bond portion.

12. A semiconductor arrangement comprising one bump electrode having two protrusions is bonded to an IC electrode on a circuit forming surface of a semiconductor element, and wherein said two protrusions are brought in contact with or put close to one electrode on a circuit board when the semiconductor element is mounted on the circuit board.

13. A semiconductor arrangement as claimed in Claim 12, wherein the electrode on the circuit board and said bump electrode are electrically connected to each other.

14. A semiconductor arrangement in which the bump electrode is bonded to an IC electrode on a circuit forming surface of a semiconductor element, and wherein

said bump electrode comprises:

a first protrusion which is comprised of a portion formed by once melting and solidifying a wire and its periphery and is bonded to said IC electrode; and

a second protrusion which is formed of an unmelted portion of said wire and extended from said first protrusion beyond a planar area defined by projecting said first protrusion on said electrode to a height approximately equal to that of said first protrusion with respect to said IC electrode, and

wherein said first protrusion and said second protrusion are brought in contact with or put close to one electrode on a circuit board when the semiconductor element is mounted on the circuit board.

15. A semiconductor arrangement as claimed in Claim 14, wherein said first protrusion is provided with a formed portion formed by forming a melted portion of said wire by a capillary and solidifying the same and a wire material portion which is comprised of the wire in a vicinity of said melted portion, extended from a vertex portion of said formed portion downwardly of said vertex portion and bonded to said formed portion.

16. A semiconductor arrangement as claimed in Claim 15, wherein said wire material portion extended downwardly from said vertex portion is bonded to said electrode, instead of said formed portion.

17. A semiconductor arrangement as claimed in Claim 14, wherein

said formed portion has a base portion bonded to said electrode and a protruding portion provided upright on said base portion.

18. A semiconductor arrangement as claimed in Claim 14, wherein said second protrusion extends toward an outer end surface side of said semiconductor element without exceeding said outer end surface.

19. A semiconductor arrangement as claimed in Claim 14, wherein said second protrusion extends outwardly of said semiconductor element beyond an outer end surface of said semiconductor element.

20. A semiconductor arrangement as claimed in Claim 14, wherein said first protrusion and said second protrusion have respective flat surface portions at the vertex portions of the protrusions.

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